Segunda tarea de diseño FPAG/VHDL de sistemas combinacionales

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3 ejercicios

**Ejercicio 1: Dos números decimales A y B en BCD, se desea ver en un 7-segmentos sólo el mayor de ellos. Si ambos resultaran iguales, no se visualizaría nada.**

Fichero vhd:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.numeric\_std.all;

use IEEE.std\_logic\_unsigned.all;

--use IEEE.std\_logic\_signed.all;

entity project\_entrega2\_1 is

port(

num\_a: in std\_logic\_vector (3 downto 0);

num\_b: in std\_logic\_vector (3 downto 0);

siete\_seg: out std\_logic\_vector (6 downto 0);

enable\_seg: out std\_logic\_vector (3 downto 0)

);

end project\_entrega2\_1;

architecture Behavioral of project\_entrega2\_1 is

signal numero: std\_logic\_vector (3 downto 0);

begin

enable\_seg <= "1110";

process(num\_a, num\_b, numero)

begin

if num\_a > num\_b then

numero <= num\_a;

elsif num\_b > num\_a then

numero <= num\_b;

else

numero <= "1111";

end if;

end process;

process(numero)

begin

case numero is

when "0000" => siete\_seg <= "1000000";

when "0001" => siete\_seg <= "1111001";

when "0010" => siete\_seg <= "0100100";

when "0011" => siete\_seg <= "0110000";

when "0100" => siete\_seg <= "0011001";

when "0101" => siete\_seg <= "0010010";

when "0110" => siete\_seg <= "0000011";

when "0111" => siete\_seg <= "1111000";

when "1000" => siete\_seg <= "0000000";

when "1001" => siete\_seg <= "0011000";

when others => siete\_seg <= "1111111";

end case;

end process;

end Behavioral;

Fichero xdc:

## Switches

set\_property PACKAGE\_PIN V17 [get\_ports {num\_b[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_b[0]}]

set\_property PACKAGE\_PIN V16 [get\_ports {num\_b[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_b[1]}]

set\_property PACKAGE\_PIN W16 [get\_ports {num\_b[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_b[2]}]

set\_property PACKAGE\_PIN W17 [get\_ports {num\_b[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_b[3]}]

#set\_property PACKAGE\_PIN W15 [get\_ports {sw[4]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[4]}]

#set\_property PACKAGE\_PIN V15 [get\_ports {sw[5]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[5]}]

#set\_property PACKAGE\_PIN W14 [get\_ports {sw[6]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[6]}]

#set\_property PACKAGE\_PIN W13 [get\_ports {sw[7]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[7]}]

#set\_property PACKAGE\_PIN V2 [get\_ports {sw[8]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[8]}]

#set\_property PACKAGE\_PIN T3 [get\_ports {sw[9]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[9]}]

#set\_property PACKAGE\_PIN T2 [get\_ports {sw[10]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[10]}]

#set\_property PACKAGE\_PIN R3 [get\_ports {sw[11]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[11]}]

set\_property PACKAGE\_PIN W2 [get\_ports {num\_a[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_a[0]}]

set\_property PACKAGE\_PIN U1 [get\_ports {num\_a[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_a[1]}]

set\_property PACKAGE\_PIN T1 [get\_ports {num\_a[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_a[2]}]

set\_property PACKAGE\_PIN R2 [get\_ports {num\_a[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_a[3]}]

##7 segment display

set\_property PACKAGE\_PIN W7 [get\_ports {siete\_seg[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[0]}]

set\_property PACKAGE\_PIN W6 [get\_ports {siete\_seg[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[1]}]

set\_property PACKAGE\_PIN U8 [get\_ports {siete\_seg[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[2]}]

set\_property PACKAGE\_PIN V8 [get\_ports {siete\_seg[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[3]}]

set\_property PACKAGE\_PIN U5 [get\_ports {siete\_seg[4]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[4]}]

set\_property PACKAGE\_PIN V5 [get\_ports {siete\_seg[5]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[5]}]

set\_property PACKAGE\_PIN U7 [get\_ports {siete\_seg[6]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[6]}]

#set\_property PACKAGE\_PIN V7 [get\_ports dp]

#set\_property IOSTANDARD LVCMOS33 [get\_ports dp]

set\_property PACKAGE\_PIN U2 [get\_ports {enable\_seg[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {enable\_seg[0]}]

set\_property PACKAGE\_PIN U4 [get\_ports {enable\_seg[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {enable\_seg[1]}]

set\_property PACKAGE\_PIN V4 [get\_ports {enable\_seg[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {enable\_seg[2]}]

set\_property PACKAGE\_PIN W4 [get\_ports {enable\_seg[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {enable\_seg[3]}]

**Ejercicio 2: Dos números decimales A y B en bcd, se desea ver en un 7-segmentos el resultado de la resta, A-B o B-A, que resulte positiva, según sea A>B o B<A, respectivamente.**

Fichero vhd:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.numeric\_std.all;

use IEEE.std\_logic\_unsigned.all;

--use IEEE.std\_logic\_signed.all;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity project\_entrega2\_1 is

port(

num\_a: in std\_logic\_vector (3 downto 0);

num\_b: in std\_logic\_vector (3 downto 0);

siete\_seg: out std\_logic\_vector (6 downto 0);

enable\_seg: out std\_logic\_vector (3 downto 0)

);

end project\_entrega2\_1;

architecture Behavioral of project\_entrega2\_1 is

signal numero: std\_logic\_vector (3 downto 0);

begin

enable\_seg <= "1110";

process(num\_a, num\_b, numero)

begin

if num\_a >= num\_b then

numero <= num\_a - num\_b;

else

numero <= num\_b - num\_a;

end if;

end process;

process(numero)

begin

case numero is

when "0000" => siete\_seg <= "1000000";

when "0001" => siete\_seg <= "1111001";

when "0010" => siete\_seg <= "0100100";

when "0011" => siete\_seg <= "0110000";

when "0100" => siete\_seg <= "0011001";

when "0101" => siete\_seg <= "0010010";

when "0110" => siete\_seg <= "0000011";

when "0111" => siete\_seg <= "1111000";

when "1000" => siete\_seg <= "0000000";

when "1001" => siete\_seg <= "0011000";

when others => siete\_seg <= "1111111";

end case;

end process;

end Behavioral;Fichero xdc:

## Switches

set\_property PACKAGE\_PIN V17 [get\_ports {num\_b[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_b[0]}]

set\_property PACKAGE\_PIN V16 [get\_ports {num\_b[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_b[1]}]

set\_property PACKAGE\_PIN W16 [get\_ports {num\_b[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_b[2]}]

set\_property PACKAGE\_PIN W17 [get\_ports {num\_b[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_b[3]}]

#set\_property PACKAGE\_PIN W15 [get\_ports {sw[4]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[4]}]

#set\_property PACKAGE\_PIN V15 [get\_ports {sw[5]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[5]}]

#set\_property PACKAGE\_PIN W14 [get\_ports {sw[6]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[6]}]

#set\_property PACKAGE\_PIN W13 [get\_ports {sw[7]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[7]}]

#set\_property PACKAGE\_PIN V2 [get\_ports {sw[8]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[8]}]

#set\_property PACKAGE\_PIN T3 [get\_ports {sw[9]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[9]}]

#set\_property PACKAGE\_PIN T2 [get\_ports {sw[10]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[10]}]

#set\_property PACKAGE\_PIN R3 [get\_ports {sw[11]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[11]}]

set\_property PACKAGE\_PIN W2 [get\_ports {num\_a[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_a[0]}]

set\_property PACKAGE\_PIN U1 [get\_ports {num\_a[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_a[1]}]

set\_property PACKAGE\_PIN T1 [get\_ports {num\_a[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_a[2]}]

set\_property PACKAGE\_PIN R2 [get\_ports {num\_a[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_a[3]}]

##7 segment display

set\_property PACKAGE\_PIN W7 [get\_ports {siete\_seg[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[0]}]

set\_property PACKAGE\_PIN W6 [get\_ports {siete\_seg[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[1]}]

set\_property PACKAGE\_PIN U8 [get\_ports {siete\_seg[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[2]}]

set\_property PACKAGE\_PIN V8 [get\_ports {siete\_seg[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[3]}]

set\_property PACKAGE\_PIN U5 [get\_ports {siete\_seg[4]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[4]}]

set\_property PACKAGE\_PIN V5 [get\_ports {siete\_seg[5]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[5]}]

set\_property PACKAGE\_PIN U7 [get\_ports {siete\_seg[6]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[6]}]

#set\_property PACKAGE\_PIN V7 [get\_ports dp]

#set\_property IOSTANDARD LVCMOS33 [get\_ports dp]

set\_property PACKAGE\_PIN U2 [get\_ports {enable\_seg[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {enable\_seg[0]}]

set\_property PACKAGE\_PIN U4 [get\_ports {enable\_seg[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {enable\_seg[1]}]

set\_property PACKAGE\_PIN V4 [get\_ports {enable\_seg[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {enable\_seg[2]}]

set\_property PACKAGE\_PIN W4 [get\_ports {enable\_seg[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {enable\_seg[3]}]

**Ejercicio 3: Tres números decimales A, B y C son introducidos mediante sendos selectores. Se desea ver en un 7-segmentos sólo el mayor de ellos.**

Fichero vhd:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.numeric\_std.all;

use IEEE.std\_logic\_unsigned.all;

--use IEEE.std\_logic\_signed.all;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity project\_entrega2\_1 is

port(

num\_a: in std\_logic\_vector (3 downto 0);

num\_b: in std\_logic\_vector (3 downto 0);

num\_c: in std\_logic\_vector (3 downto 0);

siete\_seg: out std\_logic\_vector (6 downto 0);

enable\_seg: out std\_logic\_vector (3 downto 0)

);

end project\_entrega2\_1;

architecture Behavioral of project\_entrega2\_1 is

signal numero: std\_logic\_vector (3 downto 0);

begin

enable\_seg <= "1110";

process(num\_a, num\_b, numero)

begin

if num\_a >= num\_b then

if num\_a >= num\_c then

numero <= num\_a;

else

numero <= num\_c;

end if;

else

if num\_b >= num\_c then

numero <= num\_b;

else

numero <= num\_c;

end if;

end if;

end process;

process(numero)

begin

case numero is

when "0000" => siete\_seg <= "1000000";

when "0001" => siete\_seg <= "1111001";

when "0010" => siete\_seg <= "0100100";

when "0011" => siete\_seg <= "0110000";

when "0100" => siete\_seg <= "0011001";

when "0101" => siete\_seg <= "0010010";

when "0110" => siete\_seg <= "0000011";

when "0111" => siete\_seg <= "1111000";

when "1000" => siete\_seg <= "0000000";

when "1001" => siete\_seg <= "0011000";

when others => siete\_seg <= "1111111";

end case;

end process;

end Behavioral;

Fichero xdc:

## Switches

set\_property PACKAGE\_PIN V17 [get\_ports {num\_b[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_b[0]}]

set\_property PACKAGE\_PIN V16 [get\_ports {num\_b[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_b[1]}]

set\_property PACKAGE\_PIN W16 [get\_ports {num\_b[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_b[2]}]

set\_property PACKAGE\_PIN W17 [get\_ports {num\_b[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_b[3]}]

#set\_property PACKAGE\_PIN W15 [get\_ports {sw[4]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[4]}]

#set\_property PACKAGE\_PIN V15 [get\_ports {sw[5]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[5]}]

set\_property PACKAGE\_PIN W14 [get\_ports {num\_c[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_c[0]}]

set\_property PACKAGE\_PIN W13 [get\_ports {num\_c[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_c[1]}]

set\_property PACKAGE\_PIN V2 [get\_ports {num\_c[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_c[2]}]

set\_property PACKAGE\_PIN T3 [get\_ports {num\_c[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_c[3]}]

#set\_property PACKAGE\_PIN T2 [get\_ports {sw[10]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[10]}]

#set\_property PACKAGE\_PIN R3 [get\_ports {sw[11]}]

#set\_property IOSTANDARD LVCMOS33 [get\_ports {sw[11]}]

set\_property PACKAGE\_PIN W2 [get\_ports {num\_a[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_a[0]}]

set\_property PACKAGE\_PIN U1 [get\_ports {num\_a[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_a[1]}]

set\_property PACKAGE\_PIN T1 [get\_ports {num\_a[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_a[2]}]

set\_property PACKAGE\_PIN R2 [get\_ports {num\_a[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {num\_a[3]}]

##7 segment display

set\_property PACKAGE\_PIN W7 [get\_ports {siete\_seg[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[0]}]

set\_property PACKAGE\_PIN W6 [get\_ports {siete\_seg[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[1]}]

set\_property PACKAGE\_PIN U8 [get\_ports {siete\_seg[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[2]}]

set\_property PACKAGE\_PIN V8 [get\_ports {siete\_seg[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[3]}]

set\_property PACKAGE\_PIN U5 [get\_ports {siete\_seg[4]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[4]}]

set\_property PACKAGE\_PIN V5 [get\_ports {siete\_seg[5]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[5]}]

set\_property PACKAGE\_PIN U7 [get\_ports {siete\_seg[6]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {siete\_seg[6]}]

#set\_property PACKAGE\_PIN V7 [get\_ports dp]

#set\_property IOSTANDARD LVCMOS33 [get\_ports dp]

set\_property PACKAGE\_PIN U2 [get\_ports {enable\_seg[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {enable\_seg[0]}]

set\_property PACKAGE\_PIN U4 [get\_ports {enable\_seg[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {enable\_seg[1]}]

set\_property PACKAGE\_PIN V4 [get\_ports {enable\_seg[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {enable\_seg[2]}]

set\_property PACKAGE\_PIN W4 [get\_ports {enable\_seg[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {enable\_seg[3]}]